In the Claims:

Please amend the claims as follows and add new claims 40-48:

1. (Currently Amended) An electronic component comprising:

an electronic device package [including] formed from an integral [a] silicon wafer having a recess, the recess including a conductive region; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the recess, and wherein the non-top terminal is electrically coupled to the conductive region.

2. (Previously Amended) An electronic component according to claim 1, wherein:

the conductive region is formed by metallization.

3. (Cancelled) An electronic component according to claim 2, wherein:

the metalization is achieved through a deposition process.

4. (Original) An electronic component according to claim 1, wherein the conductive region comprises:

a first layer of titanium;

a second layer of copper deposited on the first layer; and

a third layer of chrome deposited on the second layer.

5. (Original) An electronic component according to claim 1, wherein:

the device is physically coupled to the package by the conductive region.

6. (Original) An electronic component according to claim 1, further comprising:

a dielectric that is deposited so as to at least partially fill the recess.

7. (Previously Amended) An electronic component according to claim 1, further comprising:

a plurality of metallized bumps in a plane, wherein each terminal is electrically coupled to at least one bump, and each bump is electrically coupled to at most one electrically distinct terminal.

8. (Original) An electronic component according to claim 7, wherein:

the package includes a top and a bottom; and

the bumps are located above the top of the package.

9. (Previously amended) An electronic component according to claim 1, wherein the device is a vertical device and the bottom of the device is coupled to the recess.

10. (Original) An electronic component according to claim 1, further comprising:

a second conductive region coupled to a terminal other than the non-top terminal.

11. (Original) An electronic component according to claim 1, further comprising:

a plurality of contact including at least a first contact and a second contact, the first contact being electrically coupled to the non-top terminal and the second contact being electrically coupled to a terminal other than the non-top terminal.

12. (Original) An electronic component according to claim 11, wherein:

the plurality of contacts reside in the same plane.

13. (Currently Amended) An electronic component according to claim 11, further comprising:

a second layer of dielectricc completely covering the silicon [package] wafer and the device except for the plurality of contacts.

14. (Currently amended) An electronic component comprising:

an electronic component package including] formed from an integral [a] silicon wafer having a recess, the recess including a first conductive region; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal and a top terminal, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the first conductive region and the top terminal is electrically coupled to a second conductive region, and wherein at least a portion of the first and second conductive regions are essentially planar.

15. (Original) An electronic component according to claim 14, wherein: the second conductive region is a solder bump.

16. (Previously Amended) An electronic component comprising:

an electronic device package [including] formed from an integral [a] silicon wafer having a recess, the recess including a conductive region; and

an electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal located in a region other than the top of the device, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the conductive region.

17. (Original) An electronic component according to claim 16, wherein: one of the terminals of the device is a top contact located at the top of the device; and

the package has a package top, wherein the package top also includes a contact coupled electrically via the conductive region to the non-top terminal.

18. (Currently Amended) A component according to claim 16, wherein:
the conductive region comprises a layer of metal; and
the electronic device resides within the recess and the metal is electrically coupled to the non-top [bottom terminal] terminal of the device.

19. (Original) An electronic component according to claim 18, further comprising:
a layer of insulation coupling the silicon package to the electronic device.

20. (Original) An electronic component according to claim 18, wherein the metal of the conductive region extends to a portion of the package top, the electronic component further comprising:
a bottom contact electrically coupled to the metal on the package top.

21. (Currently Amended) An electronic component comprising:
an electronic device having a first terminal and a second terminal, wherein a first dimension is defined therebetween;
an electronic device package having a first surface, the package [including a] formed from an integral silicon wafer having a recess on the first surface that has a depth that is substantially equal to the first dimension, the package further having a layer of metal applied to the recess and to a portion of the first surface, wherein the electronic device resides within the recess and the second terminal is coupled to the layer of metal; and
a layer of insulation coupling the electronic device to the silicon wafer.

22. (Previously Amended) An electronic component according to claim 21, further comprising:
a first contact coupled to the first terminal; and

a second contact coupled to the metal residing on the first surface of the package.

23. (Cancelled) A method of packaging an electronic device to create an electronic component, the electronic device having a top terminal and a bottom terminal, a first dimension being defined by the distance between the top terminal and the bottom terminal, the method comprising:

creating a recess in a silicon wafer, the recess having a depth substantially equal to the first dimension of the electronic device;

applying a conductive material to the recess;

inserting the electronic device into the recess so that the bottom terminal is coupled to the conductive material;

applyin a dielectric into the recess;

applying a top contact electrically coupled to the top terminal of the electronic device; and

applying a bottom contact electrically coupled to the conductive material.

24. (Cancelled) An electronic component according to claim 23, wherein the step of applying the conductive material comprises:

applying a first layer of titanium;

applying a second layer of copper on the first layer; and

applying a third layer of chrome on the second layer.

25. (Cancelled) An electronic component according to claim 23, wherein the step of applying the dielectric into the recess comprises:

applying a dry etch bisbenzocyclobutene dielectric;

removing the dry etch bisbenzocyclobutene dielectric from the top terminal and a part of the conductive layer;

applying a photo defineable bisbenzocyclobutene dielectric; and

exposing the top terminal and the part of the conductive layer.

26. (Cancelled) The method according to claim 23, wherein:

the silicon wafer has a top and a bottom, the recess being created on a portion of the top, and wherein the bottom contact is located on the top of the silicon wafer to enable surface mounting.

27. (Cancelled) The method according to claim 26, wherein multiple recesses are created on a single silicon wafer and electronic devices are each inserted into one of the multiple recesses.

28. (Cancelled) The method according to claim 27, wherein at least one of the electronic devices is a resistor, diode, capacitor, or inductor.

29. (Cancelled) The method according to claim 27, the method further comprising:

cutting the silicon wafer to form multiple electronic components.

30. (Cancelled) The method according to claim 29, further comprising:

prior to the step of cutting, testing each of the electronic components.

31. (Cancelled) The method according to claim 23, wherein:

the electronic component is a ball grid array packaged component.

32. (Currently Amended) An electronic component comprising:

a non-molded electronic component package having a package top and formed from an integral [a] silicon wafer including a recess;

a [planar] bare die electronic device having a top, a bottom, sides, and a plurality of contacts, the device being disposed in the recess; and

a planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the package top [of the device].

33. (Cancelled) An electronic component according to claim 32, wherein:
the package is silicon.

34. (Previously Amended) An electronic component according to claim 32, further comprising:
a metallization layer.

35. (Previously Amended) An electronic component according to claim 34, wherein:
the metallization layer couples each contact to a redistribution point on the package top, and each contact remains electrically distinct.

36. (Original) An electronic component according to claim 35, further comprising:
a plurality of conductive bumps, each bump being disposed at a redistribution point.

37. (Cancelled) A method of packaging an electronic device to create an electronic component, the electronic device having a top surface and a plurality of terminals located at the top surface, the method comprising:
providing a package having a recess, the recess having a contour;
disposing the device within the recess;
mechanically coupling the device to a surface following the contour of the recess;
filling a portion of the recess not occupied by the device with a planarizing material to substantially create a level plane, wherein the plane includes the top surface of the device;
creating a plurality of redistribution points on the level plane; and
electrically coupling each of the plurality of terminals with at least one redistribution point.

38. (Cancelled) A method of packaging an electronic device to create an electronic component, the device having a device top and a plurality of terminals including a first terminal located at the device top and a second terminal located at a region other than the device top, the first and second terminals being separated by a distance defining a first dimension, the method comprising:

providing a package with a surface and a recess, the recess having a contour, wherein at least a portion of the contour extends from the surface to a depth substantially equal to the first dimension;

applying a layer of electrically conductive material to at least a portion of a surface following the contour of the recess;

disposing the device within the recess so that the second terminal is coupled to the electrically conductive region and at least a portion of the device top is substantially in the same plane as the surface of the package;

applying a first electrically conductive bump that is coupled to the first terminal; and

applying a second electrically conductive bump on the surface of the package, the bump being coupled to the electrically conductive material.

39. (Cancelled) An electronic component according to claim 38, wherein the step of applying the layer of electrically conductive material comprises:

applying a first layer of titanium;

applying a second layer of copper on the first layer; and

applying a third layer of chrome on the second layer.

40. (New) An electronic component comprising:

an electronic device package including a silicon wafer having a recess, the recess including a conductive region; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the

recess, and wherein the non-top terminal is electrically coupled to the conductive region by non-wire bonding.

41 (New) An electronic component according to claim 10 wherein the second conductive region is non-wire bonded.

42 (New) An electronic component according to claims 19, wherein the layer of insulation is a dielectric.

43. (New) The electronic component according to claim 36, such that the conductive bumps are spaced for electrically coupling with a pre-printed circuit board.

44. [New] The electronic component according to claim 43, wherein the electronic component is a flip chip.

45. [New] An electronic component comprising:

a silicon wafer having a recess;

a bare die electronic device having at least one contact, the device being disposed in the recess; and

an electrically conductive material coupling the at least one contact to an electrical input of the electronic component, wherein the electrical coupling is achieved by non-wire bonding.

46. [New] An electronic component according to claim 45, further comprising at least one layer of dielectric that resides within the recess of the silicon wafer that is not taken up by the bare die electronic device.

47. [New] An electronic component according to claim 46, wherein the bare die electronic device is covered by the dielectric material and the electronic component may be used as a flip chip.

48. [New] The electronic component according to claim 47, wherein the silicon wafer is an integral piece of silicon.